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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,966	06/21/2001	Thierry Arnaud	00GV06654266	5030

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EXAMINER

PEREZ, ANGELICA

ART UNIT	PAPER NUMBER
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2684

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/886,966

Applicant(s)

ARNAUD ET AL.

Examiner

Angelica M. Perez

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 June 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 4-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☒ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 16-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Wendelrup (Wendelrup et al.; US Patent No.: 5,943,613).

Regarding claims 16, 23 and 26, Wendelrup teaches of a process and device for reducing electrical consumption within a transmitter/receiver device (column 1, lines 12-14 and 39-50), the process comprising: generating at least one first clock signal at a first accuracy at a first power level for a transmission/reception stage and a modulator/demodulator (figure 4, item 3 and columns 1 and 2, lines 66-67 and 1-3, respectively) when the transmission/reception stage is active (column 1, lines 22-34; where transmission/reception stage is active); and generating a second clock signal at a

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second accuracy less than the first accuracy and at a second power level less than the first power level for the modulator/demodulator (figure 4, item 3 and columns 1 and 2, lines 66-67 and 1-3, respectively) when the transmission/reception stage is inactive (column 1, lines 22-34; where the "high current clock, high accuracy signal is off).

Regarding claims 17 and 27, Wendelrup teaches all the limitations of claims 16 and 26, respectively. In addition, Wendelrup teaches where generating the at least one first clock signal is generated by at least one phased-locked loop (column 5, lines 10-13).

Regarding claims 18 and 28, Wendelrup teaches all the limitations of claims 17 and 27, respectively. Also, Wendelrup teaches where the at least one phased-locked loop comprises a fractional-division phase-locked loop (columns 1 and 2, lines 40-50 and 30-35, respectively; where there are two fractional-N synthesizers).

Regarding claims 19 and 29, Wendelrup teaches all the limitations of claims 17 and 27, respectively. Also, Wendelrup teaches where the at least one phase-locked loop is inactive when the transmission/ reception stage is inactive (column 1, lines 22-34; where the transmission/ reception is inactive when the "high current clock, high accuracy signal is off; therefore, the phase-locked loop is inactive too).

Regarding claims 20 and 30, Wendelrup teaches all the limitations of claims 16 and 26, respectively. Wendelrup further teaches where the second clock signal is generated by an oscillator (figure 4, item 10).

Regarding claims 21 and 31, Wendelrup teaches all the limitations of claims 16 and 26, respectively. Wendelrup further teaches where the at least one first clock signal

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and the second clock signal are generated within a frequency synthesizer stage connected to the modulator/demodulator and the transmission/reception stage (column 1, lines 39-50 and figure 4, items 12, 10, 14, 16 and 30; e.g., interrelation among the different components).

Regarding claims 22 and 25 and 32, Wendelrup teaches all the limitations of claims 16 and 23 and 26, respectively. Wendelrup further teaches where the transmitter/receiver device is within a cellular mobile telephone (column 1, lines 31-38).

Regarding claim 24, Wendelrup teaches all the limitations of 23. In addition, Wendelrup teaches where the at least one first fractional-division phase-locked loop and said second fractional-division phase-locked loop each comprises a delta-sigma modulation fractional division phase-locked loop (column 1, lines 51-54).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 4-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wendelrup (Wendelrup et al.; US Patent No.: 5,943,613) in view of Gardner (Gardner et al.; US Patent No.: 5,950,120).

Regarding claims 4 and 7, Wendelrup teaches of a process for reducing electrical consumption of a transmitter/receiver device (column 1, lines 12-14 and 39-50) comprising a frequency synthesizer stage controlled by an automatic frequency control algorithm (column 1, lines 39-48; e.g., "control logic" where the signals at appropriate frequencies are a product of an "automatic frequency control algorithm" inherently present in an "automatic frequency control apparatus"), the process comprising: generating at least one reference signal for a transmission/reception stage within the transmitter/receiver device (column 1, lines 23-27 and 45-48; where the reference signal corresponds to the signal with the high degree of accuracy), the at least one reference signal being generated based upon at least one first fractional-division phase-locked loop within the frequency synthesizer stage (column 1, lines 23-48 where the "high degree of accuracy" corresponds to a "reference signal"); generating a clock signal based upon a second fractional-division phase-locked loop within the frequency synthesizer stage (column 1, lines 39-48);

Wendelrup does not specifically teach of generating a base signal for the at least one first fractional-division phase-locked loop and the second fractional-division phase-locked loop, the base signal having a second accuracy less than the first accuracy; and delivering the base signal as a master-clock signal to a modulator/demodulator connected to the transmission/reception stage when the transmission/reception stage and the second fractional-division phase-locked loop are inactive and delivering the clock signal as the master-clock signal when the transmission/reception stage and the second fractional-division phase-locked loop are active.

In related art concerning an apparatus and method for shutting down a wireless communication mobile station, Gardner teaches of generating a base signal for the at least one first fractional-division phase-locked loop and the second fractional-division phase-locked loop (column 8, lines 14-24; where the first and second clocks provide the reference and clock signals, respectively), the base signal having a second accuracy less than the first accuracy (column 8, lines 32-40 and 63-67; where the first and second clocks provide different accuracies; e.g., "first" and "second" accuracies); and delivering the base signal as a master-clock signal to a modulator/demodulator connected to the transmission/reception stage (column 8, lines 41-43) when the transmission/reception stage and the second fractional-division phase-locked loop are inactive (column 9, lines 9-15; where the second fractional-division phase-locked loop is active while second fractional-division phase-locked loop is inactive) and delivering the clock signal as the master-clock signal when the transmission/reception stage and the

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second fractional-division phase-locked loop are active (column 9, lines 22-27; where the first fractional-division phase-locked loop "shuts down").

It would have been obvious to a one of ordinary skill in the art at the time the invention was made to combine Wendelrup's process for reducing electrical consumption with Gardner's generating a base signal in order to complete the inherent digitalizing stage of the process.

Regarding claims 5 and 8, Wendelrup in view of Gardner teaches all the limitations according to claims 4 and 7, respectively. In addition, Wendelrup teaches where the clock signal is generated having the first accuracy (column 1, lines 23-25; where "high accuracy" corresponds to "first accuracy").

Regarding claims 6 and 15, Wendelrup in view of Gardner teaches all the limitations according to claims 4 and 7, respectively. Gardner also teaches where the transmitter/receiver device is within a cellular mobile telephone (column 1, lines 31-38).

Regarding claim 9, Wendelrup in view of Gardner teaches all the limitations according to claim 7, Gardner further teaches where the at least one first circuit comprises at least one phase-locked loop (column 5, lines 10-13).

Regarding claim 10, Wendelrup and Gardner teach all the limitations of claim 9. Wendelrup further teaches where the at least one phase-locked loop comprises a fractional-division phase-locked loop (columns 1 and 2, lines 40-50 and 30-35, respectively; where there are two fractional-N synthesizers).

Regarding claim 11, Wendelrup and Gardner teach all the limitations of claim 7. Gardner also teaches where the second circuit comprises a phase-locked loop (column 5, lines 13-15).

Regarding claim 12, Wendelrup and Gardner teach all the limitations of claim 11. Wendelrup further teaches where the phase-locked loop comprises a fractional-division phase-locked loop (columns 1 and 2, lines 40-50 and 30-35, respectively; where there are two fractional-N synthesizers).

Regarding claim 13, Wendelrup and Gardner teach all the limitations of claim 7. Wendelrup further teaches where the at least one first circuit and the second circuit are defined within a frequency synthesizer stage connected to the modulator/demodulator and the transmission/reception stage (column 1, lines 39-50 and figure 4, items 12, 10, 14, 16 and 30; e.g., interrelation among the different components).

Regarding claim 14, Wendelrup and Gardner teach all the limitations of claim 7. Wendelrup also teaches where the at least one first circuit and the second circuit are controlled by an automatic frequency control algorithm (column 1, lines 39-41; where it is inherent in the art that an automatic frequency apparatus is run by an automatic frequency control algorithm).


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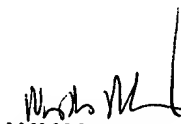
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angelica Perez whose telephone number is 703-305-8724. The examiner can normally be reached on 7:15 a.m. - 3:55 p.m., Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on 703-308-7745. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2600's customer service number is 703-306-0377.


Angelica Pérez
(Examiner)


NAY MAUNG
SUPERVISORY PATENT EXAMINER

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April 14, 2004